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Activity Report 2019

Project-Team SOCRATE

Software and Cognitive radio for telecommunications

IN COLLABORATION WITH: Centre of Innovation in Telecommunications and Integration of services

RESEARCH CENTER
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THEME
Networks and Telecommunications

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Project-Team SOCRATE

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Keywords:

Computer Science and Digital Science:

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A1.1.10. - Reconfigurable architectures
A1.1.12. - Non-conventional architectures
A1.2.5. - Internet of things
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Other Research Topics and Application Domains:

B6.2. - Network technologies
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B6.4. - Internet of things
B6.6. - Embedded systems

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2. Overall Objectives

2.1. Introduction

The success of radio networking relies on a small set of rules: *i)* protocols are completely defined beforehand, *ii)* resource allocation policies are mainly designed in a static manner and *iii)* access network architectures are planned and controlled. Such a model obviously lacks adaptability and also suffers from a suboptimal behavior and performance.

Because of the growing demand for radio resources, several heterogeneous standards and technologies have been introduced by the standard organizations or industry by different workgroups within the IEEE (802 family), ETSI (GSM), 3GPP (3G, 4G) or the Internet Society (IETF standards) leading to the almost saturated usage of several frequency bands (see Fig. 1).

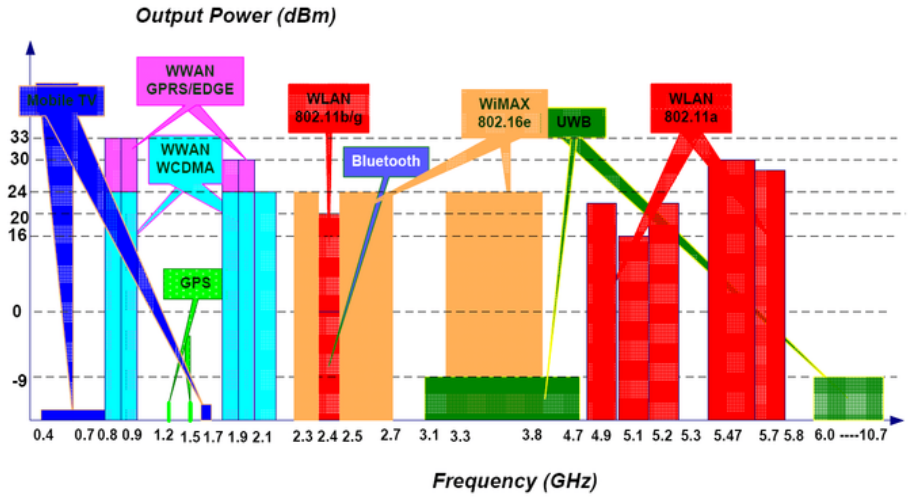

Figure 1. The most recent standards for wireless communications are developed in the UHF and VHF bands. These bands are mostly saturated (source: WPAN/WLAN/WWAN Multi-Radio Coexistence, IEEE 802 Plenary, Atlanta, USA, Nov.2007)

These two facts, obsolescence of current radio networking rules on one hand, and saturation of the radio frequency band on the other hand, are the main premises for the advent of a new era of radio networking that will be characterized by self-adaptive mechanisms. These mechanisms will rely on software radio technologies, distributed algorithms, end-to-end dynamic routing protocols and therefore require a cross-layer vision of "cognitive wireless networking": *Getting to the meet of Cognition and Cooperation, beyond the inherent communication aspects: cognition is more than cognitive radio and cooperation is not just relaying. Cognition and cooperation have truly the potential to break new ground for mobile communication systems and to offer new business models.* [37]

From a social perspective, pervasive communications and ambient networking are becoming part of more and more facets of our daily life. Probably the most popular usage is mobile Internet access, which is made possible by numerous access technologies, e.g. cellular mobile networks, WiFi, Bluetooth, etc. The access technology itself is becoming *transparent for the end user*, who does not care about how to access the network but is only interested in the services available and in the quality of this service.

Beyond simple Internet access, many other applications and services are built on the basis of pervasive connectivity, for which the communication is just a mean, and not a finality. Thus, the wireless link is expected to even be *invisible to the end user* and constitutes the first element of the Future Internet of Things [36], to develop a complete twin virtual world fully connected to the real one.

The way radio technologies have been developed until now is far from offering a real wireless convergence [26]. The current development of the wireless industry is surely slowed down by the lack of radio resources and the lack of systems flexibility.

One can get rid of this technological bottleneck by solving three complementary problems: *terminal flexibility, agile radio resource management* and *autonomous networking*. These three objectives are subsumed by the concept of *Software Radio*, a term coined by J. Mitola in his seminal work during the early 90's [33], [34]. While implementing everything in software nodes is still an utopia, many architectures now hitting the market include some degree of programmability; this is called Software-Defined Radio. The word "defined" has been added to distinguish from the ideal software radio. A software *defined* radio is a software radio which is defined for a given frequency range and a maximal bandwidth.

In parallel, the development of new standards is threatened by the radio spectrum scarcity. As illustrated in Fig. 1, the increasing number of standards already causes partial saturation of the UHF band, and will probably lead to its full saturation in the long run. However, this saturation is only "virtual" because all equipments are fortunately not emitting all the time [26]. A good illustration is the so-called "white spaces", i.e. frequency bands that are liberated by analog television disappearing and can be re-used for other purposes, different rules are set up in different countries. In this example, a solution for increasing the real capacity of the band originates from *self-adaptive behavior*. In this case, flexible terminals will have to implement agile algorithms to share the radio spectrum and to avoid interference. In this context, cooperative approaches are even more promising than simple resource sharing algorithms.

With Software-Defined Radio technology, terminal flexibility is at hand, many questions arise that are related to the software layer of a software radio machine: how will this kind of platform be programmed? How can we write programs that are portable from one terminal to another? Autonomous networking will only be reached after a deep understanding of network information theory. Thus, given that there will be many ways for transmitting data from one point to another, what is the most efficient way in terms of throughput? power consumption? etc. Last but not least, agile Radio Resource sharing is addressed by studying MIMO and multi-standard radio front-end. This new technology is offering a wide range of research problems. These three topics: software programming of a software radio machine, distributed algorithms for radio resource management and multi-standard radio front-end constitute the research directions of Socrate.

2.2. Technological State of the Art

A Software-Defined Radio (SDR) system is a radio communication system in which computations that in the past were typically implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are instead implemented as software programs [33], [29].

2.2.1. SDR Technology

The different components of a radio system are illustrated in Fig. 2. Of course, all of the digital components may not be programmable, but the bigger the programmable part (DSP/FPGA part on Fig. 2), the more *software* the radio. Dedicated IPs. In this context, IP stand for *Intellectual Properties, this term is widely used to designated dedicated special-purpose circuit blocks implemented in various technologies: Asic,* FPGA, DSP, *etc.* are needed, for these IP it is more suitable to use the term *configurable* than programmable. In a typical

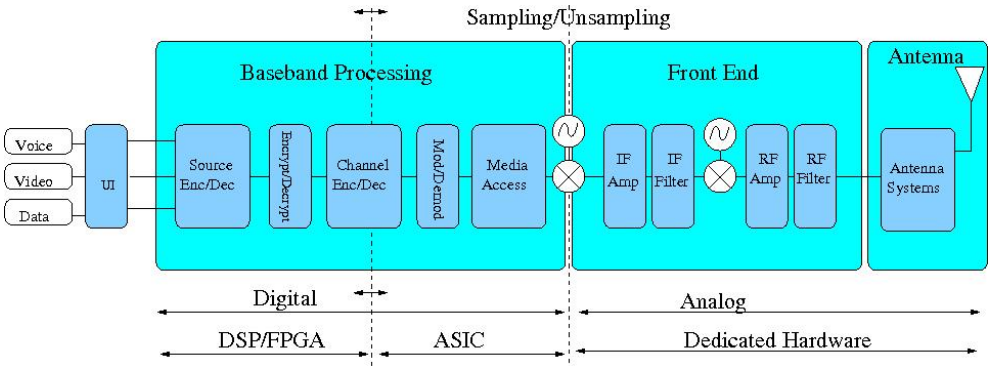

Figure 2. Radio Block Diagram, highlighting separation between digital and analog parts, as well as programmable, configurable and fixed hardware parts.

SDR, the analog part is limited to a frequency translation down to an intermediate band which is sampled and all the signal processing is done digitally.

2.2.2. SDR Forum Classification

To encourage a common meaning for the term "SDR" the SDR Forum (recently renamed *Wireless Innovation Forum* (http://www.wirelessinnovation.org) proposes to distinguish five tiers:

- *Tier 0 – Hardware Radio:* The radio parameters cannot be changed, radio is implemented only with hardware components.
- *Tier 1 – Software Controlled Radio:* A radio where only the control functions are implemented in software, baseband processing is still performed in hardware, the radio is able to switch between different hardware.
- *Tier 2 – Software-Defined Radio:* The most popularly understood definition of SDR: the radio includes software control of modulation, bandwidth, frequency range and frequency bands. Conversion to digital domain still occurs after frequency conversion. It is currently implemented using a wide range of technologies: Asics, FPGAs, DSPs, etc.
- *Tier 3 – Ideal Software Radio:* Digital conversion occurs directly at the antenna, programmability extends to the whole system.
- *Tier 4 – Ultimate Software Radio:* Same reconfigurability capabilities as in Tier 3, but with a switching between two configurations in less than one millisecond.

The main restriction to build an ideal software radio is sampling rate: sampling at a high rate is not an easy task. Following the Shannon-Nyquist theorem, sampling the RF signal at a rate greater than twice the frequency of the signal is sufficient to reconstruct the signal. Sampling can be done at lower rate (decimation), but errors can be introduced (aliasing) that can be corrected by filtering (dirty radio concept). Building an SDR terminal implies a trade-of between sampling frequency and terminal complexity. For instance, sampling at 4.9 GHz would require a 12-bit resolution ADC with at least 10GHz sample rate which is today not available with reasonable power consumption (several hundreds Watt).

2.2.3. Cognitive Radio

SDR technology enables *over the air programming* (Otap) which consists in describing methods for distributing new software updates through the radio interface. However, as SDR architectures are heterogeneous, a standard distribution method has not emerged yet.

Cognitive Radio is a wireless communication system that can sense the air, and decide to configure itself in a given mode, following a local or distributed decision algorithm. Although Tier 3 SDR would be an ideal platform for cognitive radio implementation, cognitive radios do not have to be SDR.

Cognitive Radio is currently a very hot research topic as show the dozens of sessions in research conferences dedicated to it. In 2009, the American National Science Foundation (NSF) held a workshop on "Future Directions in Cognitive Radio Network Research" [35]. The purpose of the workshop was to explore how the transition from cognitive radios to cognitive radio *networks* can be made. The resulting report indicated the following:

- Emerging cognitive radio technology has been identified as a high impact disruptive technology innovation, that could provide solutions to the *radio traffic jam* problem and provide a path to scaling wireless systems for the next 25 years.
- Significant new research is required to address the many technical challenges of cognitive radio networking. These include dynamic spectrum allocation methods, spectrum sensing, cooperative communications, incentive mechanisms, cognitive network architecture and protocol design, cognitive network security, cognitive system adaptation algorithms and emergent system behavior.

The report also mentioned the lack of cognitive radio testbeds and urged *"The development of a set of cognitive networking test-beds that can be used to evaluate cognitive networks at various stages of their development"*, which, in some sense strengthens the creation of the Socrate team and its implication in the FIT project [30].

3. Research Program

3.1. Flexible Radio Front-End

These are the research axis as they were proposed at the creation of the Socrate Team.

This axis mainly deals with the radio front-end of software radio terminals. In order to ensure a high flexibility in a global wireless network, each node is expected to offer as many degrees of freedom as possible. For instance, the choice of the most appropriate communication resource (frequency channel, spreading code, time slot,...), the interface standard or the type of antenna are possible degrees of freedom. The *multi-** paradigm denotes a highly flexible terminal composed of several antennas providing MIMO features to enhance the radio link quality, which is able to deal with several radio standards to offer interoperability and efficient relaying, and can provide multi-channel capability to optimize spectral reuse. On the other hand, increasing degrees of freedom can also increase the global energy consumption, therefore for energy-limited terminals a different approach has to be defined.

In this research axis, we expect to demonstrate optimization of flexible radio front-end by fine grain simulations, and also by the design of home made prototypes. Of course, studying all the components deeply would not be possible given the size of the team, we are currently not working in new technologies for DAC/ADC and power amplifiers which are currently studied by hardware oriented teams. The purpose of this axis is to build system level simulation taking into account the state of the art of each key component.

3.2. Multi-User Communications

While the first and the third research axes deal with the optimization of the cognitive radio nodes themselves from system and programming point of view, an important complementary objective is to consider the radio nodes in their environments. Indeed, cognitive radio does not target the simple optimization of point to point transmissions, but the optimization of simultaneous concurrent transmissions. The tremendous development of new wireless applications and standards currently observed calls for a better management of the radio spectrum with opportunistic radio access, cooperative transmissions and interference management. This challenge has been identified as one of the most important issue for 5G to guarantee a better exploitation of the spectrum. In addition, mobile internet is going to support a new revolution that is the *tactile internet*, with real time

interactions between the virtual and the real worlds, requiring new communication objectives to be met such as low latency end to end communications, distributed learning techniques, in-the-network computation, and many more. The future network will be heterogeneous in terms of technologies, type of data flows and QoS requirements. To address this revolution two work directions have naturally formed within the axis. The first direction concerns the theoretical study of fundamental limits in wireless networks. Introduced by Claude Shannon in the 50s and heavily developed up to today, Information Theory has provided a theoretical foundation to study the performance of wireless communications, not from a practical design view point, but using the statistical properties of wireless channels to establish the fundamental trade-offs in wireless communications. Beyond the classical *energy efficiency - spectral efficiency* tradeoff, information theory and its many derivations, i.e., network information theory, may also help to address additional questions such as determining the optimal rates under decentralized policies, asymptotic behavior when the density of nodes increases, latency controled communication with finite block-length theory, etc. In these cases, information theory is often associated to other theoretical tools such as game theory, stochastic geometry, control theory, graph theory and many others.

Our first research direction consists in evaluating specific mulit-user scenarios from a network information theory perspective, inspired by practical scenarios from various applicative frameworks (e.g. 5G, Wifi, sensor networks, IoT, etc.), and to establish fundamental limits for these scenarios. The second research direction is related to algorithmic and protocol design (PHY/MAC), applied to practical scenarios. Exploiting signal processing, linear algebra inspired models and distributed algorithms, we develop and evaluate various distributed algorithms allowing to improve many QoS metrics such as communication rates, reliability, stability, energy efficiency or computational complexity.

It is clear that both research directions are symbiotic with respect to each other, with the former providing theoretical bounds that serves as a reference to the performance of the algorithms created in the later. In the other way around, the later offers target scenarios for the former, through identifying fundamental problems that are interesting to be studied from the fundamental side. Our contributions of the year in these two directions are summarized further in the document.

3.3. Software Radio Programming Model

Finally the third research axis is concerned with software aspect of the software radio terminal. We have currently two actions in this axis, the first one concerns the programming issues in software defined radio devices, the second one focusses on low power devices: how can they be adapted to integrate some reconfigurability.

The expected contributions of Socrate in this research axis are :

- The design and implementation of a “middleware for SDR”, probably based on a Virtual Machine.
- Prototype implementations of novel software radio systems, using chips from Leti and/or Lyrtech software radio boards.
- Development of a *smart node*: a low-power Software-Defined Radio node adapted to WSN applications.
- Methodology clues and programming tools to program all these prototypes.

3.4. Evolution of the Socrate team

In 2018 the Socrate team which was originaly conceived to develop software defined radio has decided to split in two teams: the Maracas team will consist of the activities of Socrate Axis 2 and be directed by Jean-Marie Gorce, and the Socrate team which will consist in the Axis 1 and 3 of the current version of Socrate. This change is explicit since september 2018 as the Maracas team is created.

The advent of non-volatile memory technologies (NVRAM) is causing a major evolution in all software layers. On the one hand, the non-volatility of data in the event of a breakdown necessarily leads to fatal inconsistencies if the memory is not managed correctly. On the other hand, these memories have very different performances from the usual DRAM, which tends to the appearance of hybrid and complex memory hierarchies. Many technological and scientific challenges are to be faced in all software layers to deal with these two sets of issues. Above all, the answers to be provided depend on the calculation system considered and for what purpose it is constructed.

Within the framework of very low consumption sensors and devices, the Socrate team proposed, with Sytare [28], a software solution allowing to develop embedded applications on platforms supporting an intermittent power supply (TPS – *Transiently Powered System*) and integrating NVRAM as illustrated in Figure 3. The IPL ZEP (https://project.inria.fr/iplzep/) was also launched by Socrate last year to respond to various scientific challenges related to this issue.

The recent advance in harvesting technologies provides new research direction to Socrate which have skills in radio propagation and low power radio (wake-up radio for instance [31]. Fig 3, illustrates the *future ultra-low sensor* as envisioned by Socrate.

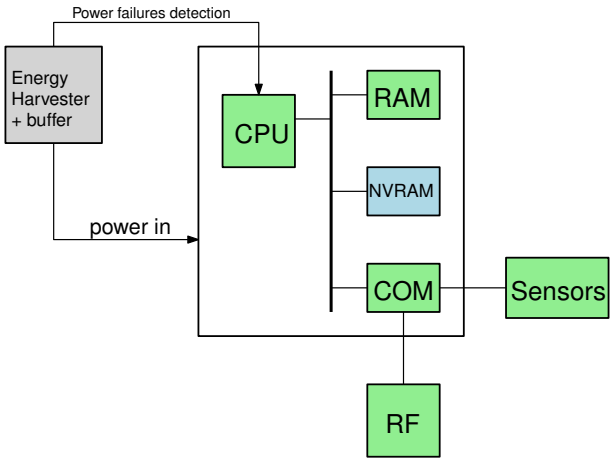

Figure 3. Architecture targeted by Socrate: low energy wireless sensor with peripherals and non volatile memory

4. New Software and Platforms

4.1. FloPoCo

Floating-Point Cores, but not only

KEYWORD: Synthesizable VHDL generator

FUNCTIONAL DESCRIPTION: The purpose of the open-source FloPoCo project is to explore the many ways in which the flexibility of the FPGA target can be exploited in the arithmetic realm.

- Participants: Florent de Dinechin and Luc Forget
- Partners: CNRS - ENS Lyon - UCBL Lyon 1 - UPVD
- Contact: Florent de Dinechin
- URL: http://flopoco.gforge.inria.fr/

4.2. Sytare

KEYWORDS: Embedded systems - Operating system - Non volatile memory

FUNCTIONAL DESCRIPTION: Sytare is an embedded operating system targeting tiny platforms with intermittent power. In order to make power failures transparent for the application, the system detects imminent failures and saves a checkpoint of program state to non-volatile memory. Hardware peripherals are also made persistent without requiring developer attention.

- Authors: Tristan Delizy, Gautier Berthou, Guillaume Salagnac, Kevin Marquet and Tanguy Risset
- Contact: Guillaume Salagnac
- Publication: Peripheral State Persistence For Transiently Powered Systems
- URL: https://hal.inria.fr/hal-01460699

4.3. NanoTracer

KEYWORDS: Embedded systems - Power monitoring - Low power consumption

FUNCTIONAL DESCRIPTION: NanoTracer is a high performance ammeter dedicated to power measurements for small devices. The system measures currents between 100nA and 100mA (gain is audo-adjusted dynamically) with a sampling frequency of 2Msps. Data is streamed to a PC over USB which enables long-running experiments, or just real-time visualization of data.

- Contact: Guillaume Salagnac
- URL: https://gitlab.inria.fr/nanotracer/

4.4. marto

Modern Arithmetic Tools

KEYWORDS: High-level synthesis - Arithmetic - FPGA

FUNCTIONAL DESCRIPTION: Marto provides C++ headers to implement custom sized arithmetic operators such as:

Custom sized posits and their environment (including the quire) Custom sized IEEE-754 numbers Custom sized Kulisch accumulators (and sums of products)

- Participants: Yohann Uguen, Florent de Dinechin and Luc Forget
- Contact: Yohann Uguen
- Publication: hal-02130912v4
- URL: https://gitlab.inria.fr/lforget/marto

4.5. hint

High-level synthesis Integer Library

KEYWORD: High-level synthesis

FUNCTIONAL DESCRIPTION: Hint is an header-only arbitrary size integer API with strong semantics for C++. Multiple backends are provided using various HLS libraries, allowing a user to write one operator and synthetize it using the main vendor tools.

- Participants: Yohann Uguen, Florent de Dinechin and Luc Forget
- Contact: Luc Forget
- Publication: hal-02131798v2
- URL: https://github.com/yuguen/hint

5. New Results

5.1. Flexible Radio Front-End

Activities in this axis could globally be divided in three main topics: wake-up radio and wireless power transfer, RFID systems and combination of spatial modulation and full-duplex.

5.1.1. Wake-Up radio and wireless power transfer

The ubiquity of wireless sensor networks (WSN), as well as the rapid development of the Internet of Things (IoT), impel new approaches to reduce the energy consumption of the connected devices. The wake-up radio receivers (WuRx) were born in this context to reduce as much as possible the energy consumption of the radio communication part. We aim at proposing a low-cost, high-efficiency rectifier to improve a quasi-passive WuRx performance in terms of communication range. By optimizing the wideband matching circuit and the proposed rectifier's load impedance, the sensitivity was increased by 5 dB, corresponding to an increase of the communication range (13 meters in free space) [10].

We also studied an original solution to maximize the DC power collected in the case of a wireless power transfer (WPT) scenario. Using state-space model representation, the WPT System is considered as a feedback approach in order to maximize the amount of harvested energy. To do this, a global simulation is performed to show the importance of taking into account the propagation channel and the rectifier circuit aspects in the case of optimizing the waveform to increase the harvested energy. By using an optimized multi-sine signal with zero phase as the excitation, taking into account the characteristics of the channel and the physical contributions of the rectifier, we managed to obtain better output DC values compared to a single tone source or a multi-sine signal without optimization, with the same average power input [14].

We plan now to apply this optimized WPT technique to feed Wireless sensors in the particular case of ventilation ducts (HVAC) [24].

5.1.2. RFID

The ARA (Auvergne Rhone Alpes) RAFTING project mainly deals with the design and analysis of wire antennas for RFID tags in the context of wearable electronics. More specifically, an helical dipole antenna dedicated to the smart textile yarn applications has been designed. Moreover, the performance was analysized with respect to mechanical constraints, together with the extraction of accurate electrical models. This work was done in collaboration with Primo 1D company. In perspective, the integration of the NFC protocol together with RFID UHF and the integration of sensing capabilities is envisaged [6], [19], [7], [12], [21].

The Spie ICS- INSA Lyon chair on IoT has granted us for a PhD thesis on Scatter Radio and RFID tag-to-tag communications. Some seminal results have shown that it is actually possible to create a communication between two RFID tags, just using ambient radiowaves or a dedicated distant radio source, without the need of generating a signal from the tag itself. Theoretical and simulated performance have been studied.

5.1.3. Combination of spatial modulation and full-duplex

Spatial modulation (SM) as a new MIMO technique is based on transmitting part of the information by activating different emitting antennas. SM increases spectral efficiency and uses only one radio frequency chain. Moreover, for full-duplex (FD) communication systems, self-interference (SI) is always a central problem. Therefore, combining FD and SM can dramatically reduce the difficulty of SIC (Self-interference Cancellation) because of the single SI chain. A Full Duplex Spatial Modulation (FDSM) system is proposed and an active analog SIC is designed in this work. Moreover, the impact of SIC accuracy on the system performance is studied. The results demonstrate that the accuracy requirement will increase as the INR (Self-interference-to-noise Ratio) increases. The FDSM system is less sensitive than the FD system, which can get a better BER (Bit Error Rate) performance as errors increase. Furthermore, an SI detector is proposed to resolve the influence of the number of detected symbols.

5.2. Software Radio Programming Model

5.2.1. Transiently powered systems and Non-Volatile Memory

Socrate is studying the new NVRAM (Non-Volatile Radom Access Memory) technology and its use in ultra-low power context. Non-Volatile memory has been extisting for a while (Nand Flash for instance) but was not sufficiently fast to be used as main memory. Many emerging technologies are forseen for Non-Volatile RAM to replace current RAM [32].

Socrate has started a work on the applicability of NVRAM for *transiently powered systems*, i.e. systems which may undergo power outage at any time. This study resulted in the Sytare software published in IEEE Transaction on Computer [3] and is also studied in an Inria Project Lab ZEP (https://project.inria.fr/iplzep/teams/).

The Sytare software introduces a checkpointing system that takes into account peripherals (ADC, leds, timer, radio communication, etc.) present on all embedded systems. Checkpointing is the natural solution to power outage: regularly save the state of the system in NVRAM so as to restore it when power is on again. However, no work on checkpointing took into account the restoration of the states of peripherals, Sytare provides this possibility.

Another acheivement in this domain is the PhD of Tristan Delizy that concerns memory heterogeneity that results from new NVM technologies. While emerging memory technologies may offer power reduction and high integration density, they come with major drawbacks such as high latency or limited endurance. As a result, system designers tend to juxtapose several memory technologies on the same chip. We aim to provide the embedded application programmer with a transparent software mechanism to leverage this memory heterogeneity. The work of Tristan Delizy studies the interaction between dynamic memory allocation and memory heterogeneity. He provides cycle accurate simulation of embedded platforms with various memory technologies and shows that different dynamic allocation strategies have a major impact on performance. He demonstrates that interesting performance gains can be achieved even for a low fraction of memory using low latency technology, but only with a clever placement strategy between memory banks. This work will soon be proposed to publication.

5.2.2. Sytare integration in Riot

The ADT SytaRiot has been granted to provide transient power management in the Riot operating system [27]. This integration was realized by Gero muller, here is a summary of the technical tasks and correponding pull request on Riot GitHub:

5.2.2.1. Port RIOT to MSP430+FRAM micro-controllers

- Bring-up the chip against the newer msp430-elf compiler and integrate the toolchain into the RIOT CI infrastructure, cf https://github.com/RIOT-OS/riotdocker/pull/67 , https://github.com/RIOT-OS/riotdocker/pull/82 , https://github.com/RIOT-OS/riotdocker/pull/91
- Implement initial support for the MSP430FR59xx in RIOT, including device drivers for key on-chip peripherals (UART, Timers, GPIO, etc). cf https://github.com/RIOT-OS/RIOT/pull/11012
- Implement a board support package for the MSP-EXP430FR5969 Launchpad Development Kit and the Boost-IR daughter-board (Infrared transceiver + keypad), cf https://github.com/geromueller/RIOT/commit/f13d33
- Participate in IETF hackathon 104 (Prague, March 23–29, 2019) to work on SUIT IoT Firmware Update, cf https://trac.ietf.org/trac/ietf/meeting/wiki/104hackathon

5.2.2.2. Explicit checkpointing in RIOT

- Implement the required low-level code (e.g. DMA driver) for saving/restoring the state of the application to FRAM. cf https://github.com/geromueller/RIOT/commits/checkpoint
- Implement save/restore methods in all relevant device drivers (DMA, GPIO, UART, Timers) and design an API to expose checkpointing as a general system service in RIOT. cf https://github.com/geromueller/RIOT/commit/8b301e

- Participate in the RIOT Summit (Helsinki, September 5–6, 2019) to give a talk about checkpointing and power measurement. cf https://summit.riot-os.org/2019/blog/speakers/gero-muller/ Power measurement

5.2.3. A high-performance ammeter for embedded systems

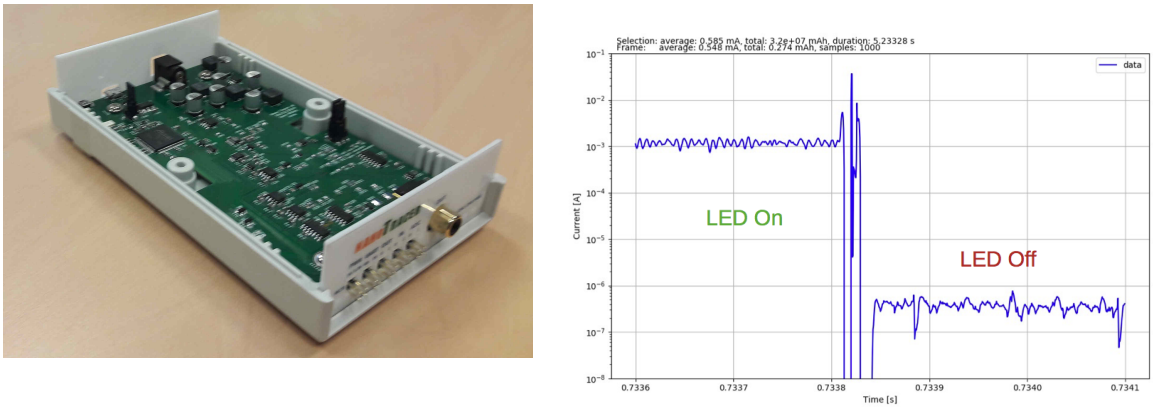

Figure 4. Photo (left) of first packaged nanoTracer prototype and snapshot (right) of a measurement provided by nanoTracer

In embedded low power processing, precise power consumption is a key issue. The Socrate team realized that existing tools could not fullfill the requirements needed for harvesting devices monitoring (measuring from nano-Amperes to milli-Ampere current values at a high sampling rate and continuously).

With the skills of Gero Müller hired on the SytaRiot ADT, the socrate team designed and built a high performance ammeter dedicated to power measurements for small devices. Our prototype measures currents between 100nA and 100mA (gain is audo-adjusted dynamically) with a sampling frequency of 2Msps. Data is streamed to a PC over USB which enables long-running experiments, or just real-time visualization of data (cf screenshot in Fig. 4).

The device, named *nanoTracer*, is referenced in the software section, it is an open project on gitlab (https://gitlab.inria.fr/nanotracer/). A first version is currently tested at Inria (Alexandre Abadie from the IoT SED team) and should soon be available for free for Inria and Academic researcher. We are working on solutions to provide a commercial circuit if requests come from other actors.

5.2.4. Ultra-low latency audio on FPGA

Recently the Socrate team started a collaboration with the researchers of the GRAME group. GRAME is a "Centre National de Création Musicale" (CNCM) organized in three departments: music production, transmission/mediation, and computer music research. Four GRAME researchers have expertise in computer science (compilation), audio DSP, digital lutherie, and human-computer interaction in general. GRAME has been leading the development of the FAUST [1] programming language since its creation in 2004. The GRAME researchers have been associated to CITI as external members in September 2019.

[1] FAUST is a domain specific language for real-time audio signal processing primarily developed at GRAME-CNCM and by a worldwide community. FAUST is based on a compiler "translating" DSP specifications written in FAUST into a wide range of lower-level languages (e.g., C, C++, Rust, Java, WASM, LLVM bitcode, etc.). Thanks to its "architecture" system, generated DSP objects can be embedded into template programs (wrappers) used to turn a FAUST program into a specific ready-to-use object (e.g., standalone, plug-in, smartphone app, webpage, etc.).

Socrate and GRAME have started a collaboration through the Syfala *(synthèse audio faible latence)* project funded by the Fédération Informatique de Lyon. The goal of Syfala is to design an FPGA-based platform for multichannel ultra-low-latency audio Digital Signal Processing (DSP), programmable at high-level with FAUST and using Socrate's software FloPoCo (http://flopoco.gforge.inria.fr). This platform is intended to be usable for various applications ranging from sound synthesis and processing to active sound control and artificial sound field/room acoustics.

Two internships have been working on this project. A first result was a presentation by Florent de Dinechin and Tanguy Risset, introducing the use of HLS and FPGA for audio, at the second *Programmable Audio Workshop* (https://faust.grame.fr/paw/) organized by GRAME.

5.2.5. Evaluation of the posit number system

The posit number system is a very elegant way to represent real numbers in a computers. Its proponents promote it as a better replacement for floating-point arithmetic: posits do indeed improve the application-level accuracy of some applications. However, this also comes with accuracy regressions in other cases. Socrate members, along with members of the AriC project-team, first studied some numerical aspects of posits [18]. Socrate then performed a thorough evaluation of the implementation of the main posit operators, improving the state of the art in hardware posit in the process. Posit operators were then compared to IEEE 754-compliant floating-point operators, and were found to be about twice as slow and twice as expensive [20], [15].

5.2.6. Evaluation of the Unum number system

CEA researcher, in collaboration with Socrate members, designed a complete accelerator for the UNUM number system, including hardware [8] and compiler support [11]. A novelty of this work is the use of a variable-length, self-describing, and memory-oriented floating-point number format [23].

5.2.7. General computer arithmetic

The 10th anniversary of the FloPoCo open-source arithmetic core generator project was the occasion to reflect on the evolutions of the field in a special session about arithmetic generator challenges organized at the ARITH conference [16].

A marked evolution over this period has been the deployment of very good High-Level Synthesis tools, thanks to which hardware is described using a software programming language (usually C++). This comes with many new arithmetic optimization opportunities, some of which have been reviewed in collaboration with Steven Derrien, from Inria Cairn [25]

An issue was the lack in this context of a portable, unified, and hardware-oriented library of arbitrary precision integers. In collaboration with David Thomas from Imperial College, London, we worked on such a library, and demonstrated that it enables a safe description of complex small-grain architectures (such as floating-point or posit operators) with a performance matching traditional hardware description languages [9].

Meanwhile, we keep studying the most basic operators. There has always existed two main methods of implementing mulitplication by a constant in hardware: Table-Based, and Shift-And-Add. This deserved a qualitative and quantitative comparison [17]. This work (with Martin Kumm, from Fulda Technical University, and Silviu Filip, from Inria Cairn) also includes a refined ILP-based algorithm for the problem of multiplying a fixed-point input number by a real constant.

6. Bilateral Contracts and Grants with Industry

6.1. Bilateral Contracts with Industry

6.1.1. Research Contract with Bosch 2019

In collaboration with Aric, Socrate worked with Bosch on the impementation of the Power function in an embedded context.

7. Partnerships and Cooperations

7.1. National Initiatives

7.1.1. Insa-Spie IoT Chair

The Insa-Spie IoT Chair http://www.citi-lab.fr/chairs/iot-chair/ relies on the expertise of the CITI Lab. The skills developed within the different teams of the lab integrate the study, modelling, conception and evaluation of technologies for communicating objects and dedicated network architectures. It deals with network, telecom and software matters as well as societal issues such as privacy. The chair will also lean on the skills developed at INSA Lyon or in IMU LabEx.

7.1.2. Inria Project Lab: ZEP

The ZEP project addresses the issue of designing tiny computing objects with no battery by combining non-volatile memory (NVRAM), energy harvesting, micro-architecture innovations, compiler optimizations, and static analysis. The main application target is Internet of Things (IoT) where small communicating objects will be composed of this computing part associated to a low-power wake-up radio system. The ZEP project gathers four Inria teams that have a scientific background in architecture, compilation, operating system and low power together with the CEA Lialp and Lisan laboratories of CEA LETI & LIST. The major outcomes of the project will be a prototype harvesting board including NVRAM and the design of a new microprocessor associated with its optimizing compiler and operating system.

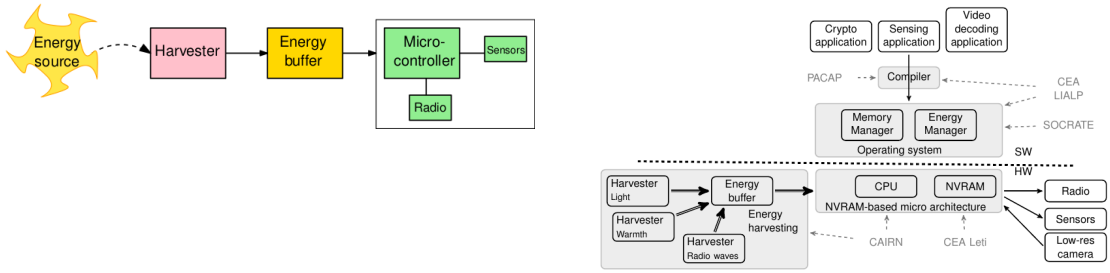

Figure 5. Example of system targeted by the ZEP project on the left, and on the right: the ZEP research program.

The scientific work (in progress) is organized around three fields :

- specific NVRAM-based architecture
- dedicated compiler pass that computes a worst-case energy consumption
- operating system managing NVRAM and energy, ensuring memory consistency across power outages

The project is illustrated by the figure 5, where PACAP, SOCRATE, CORSE, and CAIRN are the teams involved in the project.

Another important goal of the project is to structure the research and innovation that should occur within Inria to prepare the important technological shift brought by NVRAM technologies.

7.1.3. ANR - Imprenum

The objective of this project (INSA-Lyon, École Normale Supérieure de Lyon, CEA LETI) is to promote **accuracy as a first class concern** in all the levels of a computing system:

- at the hardware level, with better support for lower-than-standard and higher-than-standard precisions;
- at the level of run-time support software, in particular answering the memory management challenges entailed by adaptive precision;
- at the lower level of mathematical libraries (kernel level), for instance BLAS for linear algebra, enhancing well established libraries with precision and accuracy control;
- at the higher level of mathematical libraries (solver level, including algebraic linear solvers such as LAPACK, ad hoc steppers for Ordinary Differential Equation, eigenvalues kernels, triangularization problems for computational geometry, etc.) Here, accuracy and precision control of the lower levels should enable higher-level properties such as convergence and stability;
- at the compiler level, enhancing optimising compilers with novel optimisations related to precision and accuracy;
- at the language level, embedding accuracy specification and control in existing languages, and possibly defining domain-specific languages with accuracy-aware semantics for some classes of applications.

7.1.4. ADT SytaRiot

The Riot system (https://www.riot-os.org/) is well known within Inria, it is a joint implementation of Inria and Freie Universität Berlin which is today one of the most widely used open-source OS on small embedded systems. The arrival of non-volatile memories promises a new generation of sensors on which the memory hierarchy will be more heterogeneous than today. The communicating system will be able to undergo a power cut em complete and resume its current activity when power returns.

Sytare (https://gitlab.inria.fr/citi-lab/sytare/), developed for three years by the Socrates team (with the support of an ADT), targets intermittent feeding which will arrive when the technologies of *harvesting* (recovery of ambient energy) are democratized.

The objective of this ADT is to make Riot compatible with NVRAM-based architecture, therefore to integrate Sytare with Riot and thus open Riot to ultra low power platforms containing NVRAM, *eg* Texas microcontrollers Instrument MSP430FR5969.

7.1.5. Digital Hardware AI Architectures

Florent de Dinechin participates to the chair *Digital Hardware AI Architectures* held by Prof. Frédéric Pétrot at the Multidisciplinary Institute in Artificial Intelligence (MIAI) of Grenoble. The other participants are François Duhem (Spintec/CEA) and Fabrice Rastello (LIG/Inria), with industrial partners Google France, Kalray, STMicroelectronics, and Upmem.

This chair funds the PhD of Maxime Christ, which studies how very low-precision arithmetic formats may improve the efficiency of the learning phase of neural networks.

7.2. European Initiatives

7.2.1. Collaborations in European Programs, Except FP7 & H2020

Socrate is very active in COST IRACON CA15104: Guillaume Villemaud is National Delegate (Alt.) and FIT/CorteXlab is identify as one of the COST platform.

7.3. International Initiatives

7.3.1. Inria International Partners

7.3.1.1. Informal International Partners

Socrate has collaborations with the following international partners.

- **University of Cyprus**, Department of Electrical and Computer Engineering, University of Cyprus, Nicosia, Cyprus. This cooperation with Prof. Ioannis Krikidis is on topics related to energy-harvesting and wireless communications systems. Scientific-Leaders at Inria: Guillaume Villemaud.
- **Universidad Nacional del Sur**, LaPSyC laboratory, Bahía Blanca , Argentina. This cooperation with Prof. Juan Cousseau is on topics related to Full-Duplex communications and Interference Alignment. Scientific-in-charge at Inria: Guillaume Villemaud.
- **Technical University "Gh. Asachi" of Iasi, Romania**, Department of Electronics, Telecommunications and Information Technology. This recent collaboration has started on topics related on the theoretical aspects of the ultra-low power radio communications. Scientific-in-charge at Inria: Florin Hutu
- **Technical University of Fulda, Germany**. This collaboration with the group of Martin Kumm covers many aspects of computer arithmetic, with several joint papers, collaboration on the FloPoCo project, and work in progress on a textbook to appear in 2020. Scientific-in-charge at Inria: Florent de Dinechin
- **Imperial College, London, UK**, departments of Computing and Electrical Engineering. This collaboration with the groups of David Thomas and George Constantinides covers several aspects of reconfigurable computing and reconfigurable arithmetic. Scientific-in-charge at Inria: Florent de Dinechin

8. Dissemination

8.1. Promoting Scientific Activities

8.1.1. Scientific Events: Organisation

Tanguy Risset and Leonardo Cardoso have been at the origin ot the First French GNU Radio days in 2018: https://gnuradio-fr-18.sciencesconf.org/. This is a very visible result of the activity on CorteXlab. The second version of the workshop (called now *european GNU Radio days*) has almost double its number of participants in 2019: https://gnuradio-fr-19.sciencesconf.org/. Next year session is planned in June in Poitier.

Kevin Marquet has organized the conference “Vous avez dit sobriété (numérique) ?” within the Ecoinfo CNRS GDS (https://ecoinfo.cnrs.fr/2019/07/11/projets-ecoinfo-en-cours/).

8.1.1.1. Member of the Organizing Committees

- Tanguy Risset is member of the organizing committee of the second European GNU Radio days.

8.1.1.2. Chair of Conference Program Committees

Florin Hutu was session chair during the IEEE International Symposium on Signals Circuits and Systems, 11-12 July 2019, Iasi, Romania.

8.1.1.3. Member of the Conference Program Committees

Tanguy Risset was a member of the following technical program committees:

- IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2019
- Design Automation and Test in Europe (DATE) 2019
- International Conference on Cognitive Radio Oriented Wireless Networks (CROWNCOM) 2019

Florent de Dinechin was a member of the following technical program committees:

- IEEE Symposium on Computer Arithmetic (ARITH)
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)
- Conférence d'informatique en Parallélisme, Architecture et Système (COMPAS)

Guillaume Villemaud was a member of the following technical program committee:

- EUCAP 2019,
- EuCNC 2019

8.1.2. Journal

8.1.2.1. Member of the Editorial Boards

Guillaume Villemaud is an associate editor of Annals of Telecommunications (Springer).

Florent de Dinechin was Guest Editor for a special issue of IEEE Transactions on Computers dedicated to computer arithmetic [4].

8.1.2.2. Reviewer - Reviewing Activities

Florin Hutu reviewed articles for the following conferences: 2019 International Conference on Advanced Technologies for Communications (ATC), 2019 IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC),

Florin Hutu Florin HUTU reviewed articles for the following journals: IEEE Transactions on Communications, IEEE Communications Letters, IEEE Journal of Radio Frequency Identification, Elsevier Advances in Space Research, MDPI Sensors, MDPI Applied Sciences.

8.1.3. Invited Talks

Florent de Dinechin gave a talk at the PAW workshop (Programmable Audio Workshop) organised by GRAME in Lyon on 14 dec. 2019. the title was: "FPGAs for low latency audio applications?" (https://faust.grame.fr/paw/#fpga)

Florent de Dinechin gave an invited lecture at ICTP (the International Center for Theoretical Physics) for the May 2019 edition of the Advanced Workshop on FPGA-based Systems-On-Chip for Scientific Instrumentation and Reconfigurable Computing.

Tanguy Risset gave a tutorial untitled "Writing a custom GNU Radio processing block"at the second edition of the *european GNU Radio days*, organized in besançon in June 2019 (https://gnuradio-fr-19.sciencesconf.org/resource/page/id/2).

Gero Müller gave an invited talk untitled "Intermittent power and high precision high speed power measurements" at Riot Summit 2019 (https://summit.riot-os.org/2019/blog/speakers/gero-muller/)

8.1.4. Leadership within the Scientific Community

Tanguy Risset is Vice-director of the FIL (CNRS Computer Science Research Federation of Lyon/Saint-Etienne).

Florent de Dinechin is director of the Citi-Lab.

8.1.5. Scientific Expertise

Guillaume Villemaud served as Research Expert for the European commission for the H2020-MSCA-NIGHT-2018.

Tanguy Risset is member of the Administration council (Conseil d'administration) of the GRAME institute (centre national de création musicale).

Guillaume Villemaud is a member of the Delphi Expert Panel on Software Defined Networks (SDN) and Network Functions Virtualisation (NFV).

8.1.6. Research Administration

Tanguy Risset is Vice-director of the FIL (CNRS Computer Science Research Federation of Lyon/Saint-Etienne).

Florent de Dinechin is director of the Citi-Lab.

Kevin Marquet is associate director of the CNRS GDS ECO-info (http://ecoinfo.cnrs.fr/)

8.2. Teaching - Supervision - Juries

8.2.1. Teaching

- Tanguy Risset is professor at the Telecommunications Department of Insa Lyon.
- Florent de Dinechin is a professor at the Computer Science Department of Insa Lyon. He also teaches computer architecture at ENS-Lyon.
- Guillaume Salagnac and Kevin Marquet are associate professors at the Computer Science Department of Insa Lyon.
- Guillaume Villemaud and Florin Hutu are associate professor at the Electrical Engineering Department of Insa Lyon.

8.2.2. Supervision

PhD in progress : **Gautier Berthou** : *Operating system for transiently powered systems*, Inria, (IPL ZEP) since 01/2018.

PhD in progress : **Andrea Bocco** : *Proposition d'une unité de caclul UNUM pour le calcul scientifique*, ANR Metalibm grant, since 12/2016.

PhD in progress : **Luc Forget** : *Algèbre linéaire calculant au plus juste*, ANR Imprenum, since 10/2018.

PhD in progress :**Yanni Zhou** : *Full Duplex and spatial modulation* since 10/2018

PhD in progress : **Tarik Lassouaoui** : *Tag 2 Tag communication* since 10/2018

PhD in progress : **Regis Rousseau** : *Wireless Power Transfer* since 10/2018

PhD starting : **Maxime Christ** : *Learning in Very Low Precision* since 10/2018

PhD defended : **Yohan Uguen** : *High-level synthesis and arithmetic optimizations*, École Doctorale MathInfo,Nov. 2019.

PhD defended : **Tristan Delizy** : *Gestion de la mémoire dynamique pour les systèmes embarqués avec mémoire hétérogène*, École Doctorale MathInfo, Dec. 2019.

8.2.3. Juries

- Tanguy Risset was a member of the jury of the these following theses:
  - Arthur Hugeat (U. Bourgogne Franche-comté)
  - Tristan Delizy (U. Lyon)
- Tanguy Risset was a member of the jury of the HDR of Matthieu Gautier (U. Rennes)
- Florent de Dinechin was a reviewer for
  - the PhD of Geneviève Ndour (U. Rennes 1)
  - the PhD of Yohan Chatelain (U. Paris Saclay)

8.3. Popularization

8.3.1. Education

Florent de Dinechin gave a lecture in Grenoble for high-school teachers, in the framework of the ISN convention between Académie de Grenoble and Inria.

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Invited Conferences

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